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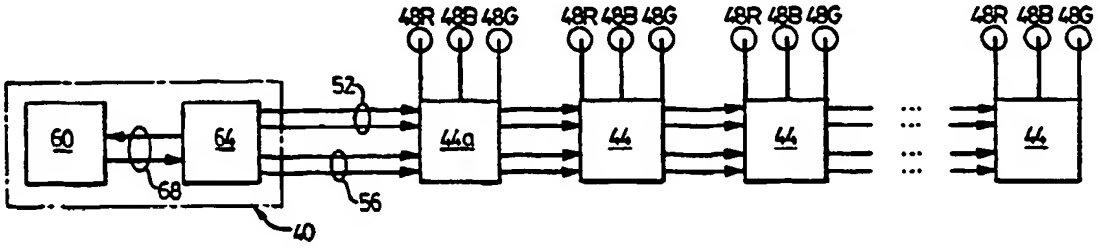

(57) Abstract

A controlled lighting comprises a control system which transmits DATA and CLOCK information to a plurality of light modules. The light modules each include at least two light elements and a control unit which is responsive to the DATA and CLOCK information received from the control system to vary individually the amount of light emitted by each of the light elements in each light module. Contemplated uses of the controlled lighting system include decorative lighting, illuminated display signs, etc.

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Controlled Lighting System

TECHNICAL FIELD

The present invention relates to lighting systems. More particularly, the present invention relates to controlled lighting systems including light elements which are controlled from a remote location.

BACKGROUND ART

Controlled lighting systems are known. Such systems typically comprise a series of light elements wherein the power supplied to each light element is controlled from a remote location. The power supplied is varied to change the amount of light produced by the light elements as desired.

A prior art controlled lighting system of interest is shown in U.S. Patent Re. 32,341 to Smith. This reference shows a lighting system for a discotheque which comprises a plurality of white light elements which are arranged in a circle and which may be illuminated or extinguished in predefined patterns to provide various lighting effects. Each light element in the system has a power module associated with it which receives signals from a remote control unit to illuminate or extinguish the light element as desired.

Another prior art controlled lighting system of interest is shown in U.S. Patent 4,317,071 to Murad. This reference shows a system for decoratively lighting a fountain or the like. Three lighting circuits are each connected directly to one or more light elements of a particular colour. In response to a pre-programmed input or to a music input, the system alters the degree of illumination of the lighting circuits.

However, problems exist with these and other prior art controlled lighting systems of which the present inventor is aware. One problem is the cost associated with providing a control unit for each light element in the system. This cost limits the range of applications in which the prior art controlled lighting systems may effectively be employed. Further, prior art controlled lighting systems do not allow a range of colours and brightness levels to be produced by light elements which are controlled from a remote location.

DISCLOSURE OF THE INVENTION

It is an object of the present invention to provide a novel controlled lighting system which obviates or mitigates at least some of the disadvantages or problems with the prior art.

According to one aspect of the present invention, there is provided a controlled lighting system comprising: a control system; a plurality of light modules, each module including at least two light elements; a control unit for each light module receiving control signals from said control system and independently operating each of said at least two light elements in response to said control signals, each control unit operating in response to a unique control signal.

According to another aspect of the present invention, there is provided a light module comprising: a housing; at least two light elements within said housing, each light element emitting light of a different wavelength; means to blend the light emitted by each said light element; a control unit responsive to signals to vary the light emitted by each said light element.

According to yet another aspect of the present invention, there is provided an illuminated display comprising: a support; a control system; a plurality of light modules arranged in an array on said support, each light module including at least two light elements and a control unit to independently alter the amount of light emitted by each of said light elements in response to control signals received from said control system, wherein said control system transmits a predefined sequence of control signals to said light modules to illuminate said light elements of said light modules to produce a desired display.

BRIEF DESCRIPTION OF THE DRAWING

Preferred embodiments of the present invention will now be described, by way of example only, with reference to the attached figures wherein:

Figure 1 shows a block diagram of a controlled lighting system in accordance with the present invention;

Figure 2 shows a block diagram of a transmitter for the controlled lighting system of Figure 1;

Figure 3 shows a schematic diagram of the transmitter of Figure 2;

Figure 4 shows a block diagram of a control unit for the controlled lighting system of Figure 1;

Figure 5 shows a schematic diagram of a portion of the control unit of Figure 4;

Figure 6 shows a schematic diagram of another portion of the control unit of Figure 4;

Figure 7 shows a front view of a light module for use in the controlled lighting system of Figure 1;

Figure 8 shows a side view of the light module of Figure 7;

Figure 9 shows a top view of a control unit portion of the light module of Figure 7; and

Figure 10 shows an illuminated display sign constructed from the controlled lighting system of Figure 1.

BEST MODE FOR CARRYING OUT THE INVENTION

Figure 1 shows a block diagram of a lighting system in accordance with the present invention. The system includes a control system 40 and a plurality of control units 44, each of which includes at least two light elements 48. In the embodiment shown, each control unit 44 includes a light element 48R which emits red light, a light element 48G which emits green light and a light element 48B which emits blue light.

Control units 44 are connected in series fashion to control system 40 by two pairs of electrical connectors 52 and 56. Connectors 52 supply dc power to each control unit 44 to operate the control units and to power light elements 48. As will be described in further detail below, connectors 56 supply CLOCK and DATA command signals to control units 44 from control system 40.

Control system 40 comprises a controller 60 and a transmitter 64. In the embodiment shown, controller 60 is a microcomputer such as an IBM PC which is connected to transmitter 64 through a standard Centronics parallel port 68. As will be apparent to those of skill in the art, other controllers, such as dedicated microprocessor-based controllers, may be employed as desired. Controller 60 provides control data, which may be derived from a program, to control units 44 as described below. Additionally, the controller 60 may supply control data which has been modified by appropriate sensor input. For

example, controller 60 may respond to a light sensor to reduce the brightness of light elements 48 in low ambient lighting conditions and to increase the brightness of light elements 48 in high ambient lighting conditions.

Transmitter 64 is shown in block diagram form in Figure 2 and schematically in Figure 3. Transmitter 64 comprises six different functional blocks: Parallel to Serial Converter 72; Logic Control 76; Pulse Generator 80; Pulse Counter & Divider 84; Power-Up Reset 88; and Voltage Converter 92.

In the embodiment shown, transmitter 64 is implemented from standard TTL components, such as those described in "The TTL Logic Data Book" published by Texas Instruments Incorporated. It will be apparent that other implementations are possible, including application specific integrated circuits (ASICs).

Pulse Generator 80 comprises IC25 which is a 74LS123 Retriggerable Monostable Multivibrator configured to provide a square wave timing signal to Pulse Counter & Divider 84 at approximately 2 MHz.

Pulse Counter & Divider 84 comprises IC22 which is a 4-Bit Binary Counter such as a 74LS93, IC23 and IC24 which are 74LS74 D-Type Flip-Flops, one gate of IC27 which is a 74LS00 2-input NAND gate and one gate of IC28 which is a 74LS09 2-input AND gate. Pulse Counter & Divider 84 receives the square wave timing signal from Pulse Generator 80 and divides the frequency by two to improve its stability. The divided signal is employed as a square wave CLOCK signal further described below. Pulse Counter & Divider 84 also operates to count the

pulses on the CLOCK signal to a count of 8 pulses and to a count of 10 pulses. The use of these two counts are described below.

Parallel to Serial Converter 72 includes a 74LS165 parallel load 8 bit shift register IC21. IC21 is connected to the eight data lines of parallel port 68 and transforms the 8 bits of parallel data into a serial data stream of bits in response to 8 pulses received from Pulse Counter & Divider 84. The serial data bits are output on the DATA line to Voltage Converter 92.

Voltage Converter 92 comprises IC30 which is a MC1488 line driver, manufactured by Motorola. IC30 converts the voltage levels on the DATA line from Parallel to Serial Converter 72 and the voltage levels on the CLOCK line from Pulse Counter & Divider 84 from standard 0 and 5 volt TTL voltage levels to -12 and +12 volts. The conversion to the -12 and +12 voltage levels provides signals which are better suited for transmission over substantial distances to control units 44.

Power-Up Reset 88 is an analog network comprising T4 which is a 2N4400 transistor, D6 which is a 1N4148 diode, C11 which is a 4.7 microfarad capacitor and R9 which is a 22 Kohm resistor. As will be apparent to those of skill in the art, when transmitter 64 is powered up Power-Up Reset 88 provides a reset pulse to place transmitter 64 into a predefined known state.

Logic Control network 76 provides the 'handshaking' required by parallel port 68. Logic Control network 76 comprises IC23 and IC24 which are described above, gates from IC26 and IC27 which are 74LS00 2-input NAND gates, gates from IC28 which is described above, and

gates from IC29 which is a 74LS32 2-input OR gate. On receipt of the STROBE signal from parallel port 68, Logic Control network 76 sets IC21 to load the 8 bits of parallel data from parallel port 68 into its internal shift register and sets Pulse Counter & Divider 84 to commence counting.

On each count of Pulse Counter & Divider 84, IC21 outputs one bit of data onto the DATA line and one bit of clock data onto the CLOCK line to Voltage Converter 92. When Pulse Counter & Divider 84 has reached a count of 8, further output from Parallel to Serial Converter 72 to the DATA line is inhibited but two additional bits of clock data are output onto the CLOCK line until Pulse Counter & Divider 84 reaches a count of 10. As will be described below, at control units 44 the ninth CLOCK bit acts as a data latch bit and the tenth bit acts as a reset bit.

Once Pulse Counter & Divider 84 has reached a count of ten, Logic Control 76 asserts the INTERRUPT signal to parallel port 68 to indicate that transmitter 64 is ready to receive another 8 bits of data from parallel port 68 and the transmission cycle may start again.

As will be further described below, in the illustrated embodiment control signals are transmitted to control units 44 in the form of one of three different 8-bit 'words'. The first word is in the form "dddddd11", where 'dddddd' represents 6 bits of address data and the trailing '11' identifies the data as being a group address ID. The second word is in the form "dddddd01", where 'dddddd' represents 6 bits of address data and the trailing '01' identifies the data as being a unit address ID. The third word in the form "xxxdddd0" where the three initial x's indicate which light element the data relates to, the 'dddd' represents the binary

value for the light(s) and the trailing 0 indicates that the word is a light data word.

In the embodiment shown, a one in the leading 'x' selects light element 48R, a one in the second 'x' selects light element 48B and a one in the trailing 'x' selects light element 48G. Of course, two or more light elements can be selected at the same time to receive the same binary data by setting more than one 'x' to one. It is contemplated that this will be useful in many circumstances, such as extinguishing or illuminating all of the light elements of a particular module at the same time.

Control unit 44 will now be described with reference to Figure 4, which shows a block diagram of control unit 44, and to Figures 5 and 6 which show schematic diagrams thereof. In Figures 5 and 6, the interconnections between the two diagrams are indicated by the tabs labelled A through K.

As can be seen in Figure 4, each control unit 44 comprises six main function blocks as well as a Gate Amplifier 90 and the three D/A Converter and Drivers 94R, 94B, 94G. A Voltage Conversion block 96 is also included for the control unit 44 which is closest electrically to control system 40 as will be further described below.

The six main function blocks comprise Data Transmission Logic Control 100, Serial to Parallel Converter 104, Power-Up Reset 108, Data Register Control Logic 112, Address Decoder Block 116 and Data Register Block 120. As can be seen, Address Decoder Block 116 includes a Group ID Decoder 124 and a Unit ID Decoder 128. Further,

Data Register Block 120 includes three Data Registers 132R, 132B, 132G.

In the embodiment shown in Figures 5 and 6, control unit 44 is implemented from standard TTL components. It is contemplated that, in some uses of the present invention such as for decorative lighting, other implementations will be preferred for convenience and/or economy. Such other implementations will be apparent to those of skill in the art and include, but are not limited to, application specific integrated circuits (ASICs) and/or gate arrays.

As discussed above, control units 44 are connected in series fashion to control system 40. The control unit 44a which is electrically closest to control system 40 includes Voltage Conversion block 96 which transforms the -12V and +12V voltage levels of the CLOCK and DATA signals on electrical connectors 56 from control system 40 to standard TTL voltage levels of 0 and +5V respectively. As shown in Figure 5, Voltage Conversion block 96 comprises IC15 which is a MC1489AD voltage mode receiver, manufactured by Motorola and two gates of IC19 which is a 74LS04 hex inverter. Once converted to 0 and +5V levels, the CLOCK and DATA signals are applied to Data Transmission Logic Control 100 and to Serial/Parallel Conversion 104 respectively.

The remaining control units 44 which are electrically further from control system 40 do not require a Voltage Conversion block 96 as they receive their CLOCK and DATA signals on electrical connectors 56 via the electrically preceding control unit's Gate Amplifier 90 which outputs 0 and 5V level signals. Each Gate Amplifier 90 regenerates the CLOCK and DATA signals to minimize degradation of the signals for each following control unit 44. Gate Amplifier 90 comprises two gates of

IC8 which is a 74LS32 OR Gate. Two 5.1V Zener diodes D2 and D3 are employed to remove over-voltage spikes on the DATA and CLOCK lines. It will be apparent that the Gate Amplifier 90 may be omitted from the control unit 44 which is electrically most distant from control system 40 if desired.

Regardless of whether Voltage Conversion block 96 or the Gate Amplifier 90 of an electrically preceding control unit supplies the 0V and 5V CLOCK and DATA signals, the electrical circuitry of each control unit 44 is powered by the 5V dc voltage supplied through electrical connecters 52. To ensure correct voltage levels to each control unit 44, each control unit includes IC14 which is a LM78M05 positive voltage regulator.

Data Transmission Logic Control 100 comprises two more gates of IC8, described above, three gates of IC9 which is a 74LS00 2-Input NAND Gate, IC10 which is a 74LS93 4-bit Binary Counter and IC13 which is a 74LS74 D-Type Flip Flop. Data Transmission Logic Control 100 controls the serial to parallel data conversion and, as will be further described below, provides a data latch pulse and a reset pulse.

Serial/Parallel Converter 104 comprises IC12 which is a 74LS164 8-Bit Parallel-Out Shift Register. Data Transmission Logic Control sets Serial/Parallel Converter 104 to load one bit of serial data from the DATA line for each of eight CLOCK pulses, whether the DATA and CLOCK pulse are received from Voltage Conversion block 96 or from the Gate Amplifier 90 of a preceding controller 44.

Group ID Decoder 124 of Address Decoder block 116 comprises six gates of IC16 which is a 74LS04 inverter and IC17 which is a 74LS30 8-Input NAND gate.

As shown in Figure 5, the least two significant output bits of IC12 are directly connected to two of the inputs of IC17 (labelled G and C in the Figure). As described above, a data word representing a Group ID has its two least significant bits set to '11' and these two bits are effectively tested by IC17 to determine whether of not the data word is a Group ID. The remaining inputs to IC17 may be connected by jumpers 100 either directly or through inverter gates of IC16 to the remaining output bits of IC12 which constitute the data bits.

By setting jumpers 100 in a particular manner, any one of up to sixty four Group ID's may be selected. In Figure 5 a Group ID of three (binary "000011") has been selected for control unit 44 by setting jumpers 100E and 100F to directly connect two inputs of IC17 to the two least significant data bits of IC12 while the remaining jumpers 100A through 100D have been placed to connect IC12 to IC17 through inverter gates of IC16.

Unit ID Decoder 128 of Address Decoder block 116 comprises six gates of IC7 which is a 74LS04 inverter, one gate of IC19 which is also a 74LS04 inverter and IC11 which is a 74LS30 8-Input NAND gate.

The least significant output bit of IC12 (labelled C) is directly connected to one input of IC11 while the next least significant bit of IC12 (labelled G) is connected to another input of IC11 through an inverter gate of IC19. As described above, a data word representing a

Unit ID has its two least significant bits set to '01' and these two bits are effectively tested by IC11 to determine whether of not the data word is a Unit ID.

The remaining inputs to IC11 may be connected by jumpers 104 either directly or through inverter gates of IC7 to the remaining output bits of IC12 which constitute the data bits. As with Group ID Decoder 124 described above, by setting jumpers 104 in a particular manner, any one of up to sixty four Unit ID's may be selected. In Figure 5 a Group ID of eight (binary "001000") has been selected for control unit 44 by setting jumper 104C to directly connect an input of IC11 to the third most significant data bit of IC12 while the remaining jumpers 104A, 104B, 104D, 104E and 104F have been placed to connect outputs of IC12 to inputs of IC11 through inverter gates of IC7.

The above-described Address Decoder block 116 is has been designed to allow for a plurality of light modules to be attached to a single control system 40. In fact, with the capacity for sixty-four different Group IDs and sixty-four Unit IDs, the above-described Address Decoder block 116 provides for up to four thousand and ninety six uniquely addressed light modules to be connected to a single control system 40. It will be apparent to those of skill in the art that in some circumstances, more or fewer numbers of unique addresses will be required and Address Decoder block 116 may be modified accordingly. For example, in a system requiring less than one hundred and twenty eight unique addresses, Group ID Decoder 124 may be removed and Unit ID Decoder 128 and Data Register Control Logic 112 modified accordingly.

Data Register Control Logic 112 comprises both gates of IC4 and IC5 which are 74LS21 4-Input AND gates, IC6 which is a 74LS04 Inverter, IC13 and IC18 which are 74LS74 D-Type Flip-Flops, one gate of IC9 described above and one gate of IC19 described above.

Power-Up Reset 108 comprises an analog network of T4 which is 2N4400 transistor, C1 which is a 2.2 microfarad capacitor, D1 which is a 1N4148 diode, and R1 which is a 2.4kOhm resistor. As will be apparent to those of skill in the art, Power-Up Reset 108 operates to supply a reset pulse upon power-up of control unit 44 to place the control unit into a known state.

As shown in Figure 6, each of D/A Converter and Drivers 94R, 94B, 94G comprises a 74LS75 4-Bit Bi-Stable Latch (IC1, IC2 and IC3 respectively). Resistors R1 through R4 (2.4 Kohms, 1.2 Kohms, 560 ohms and 390 ohms respectively) are connected to the outputs of the 74LS75 and with R6 (5.1 Kohms) and R5 (560 ohms) act as a D/A converter to control a 2SC1096 Driver Transistor (T1, T2 and T3 respectively) which drives its associated light element 48R, 48B, 48G. As will be understood by those of skill in the art, depending upon which and how many outputs of 74LS75 are set to +5V, the brightness of the associated light element 48 will be varied accordingly.

Operation of a control unit 44 will now be described by way of example. Data Transmission and Logic Control 100 receives CLOCK signals from electrical connecter 56 and causes Serial/Parallel Conversion unit 104 to load eight bits of DATA from electrical connecter 56 and convert it into a word of data.

If the two least significant bits of the received word are '11', Group ID Decoder 124 checks to see if the Group ID received matches that of the control unit 44 as set by jumpers 100. If the Group ID does not match, the received word of data is ignored as it is intended for another control unit 44. If the Group ID does match, on the ninth (data latch) CLOCK pulse, Data Register Control Logic 112 is set to receive the Unit ID. The tenth (reset) CLOCK pulse received clears IC10 and IC12 in preparation to receive the next eight DATA bits.

The next eight DATA bits are received during the next eight CLOCK pulses and are converted to an eight bit data word. Provided that the two least significant bits of the received word are '01', Unit ID Decoder 128 checks to see if the Unit ID received matches that of the control unit 44 as set by jumpers 104. If the Unit ID does not match, the received word of data is ignored as it is intended for another control unit 44. If the Unit ID does match, on the ninth (data latch) CLOCK pulse, Data Register Control Logic 112 asserts the SELECT line to Data Registers 132 and one the tenth (reset) CLOCK pulse, IC10 and IC12 are cleared in preparation to receive the next eight DATA bits.

The next eight data bits are received during the next eight CLOCK pulses and are converted into an eight bit data word as before. Provided that the least significant bit (bit 8) of the word is set to '0', this received word comprises lamp control data.

On the ninth (data latch) CLOCK pulse the STROBE PULSE signal is asserted by Data Register Control Logic 112 and, if the most significant bit of the word (bit 1) is set to '1', the four bits of data at bits 4, 5, 6 and 7 will be loaded into Data Register 120R. Alternatively, if the second or third bits (bit 2 or bit 3) of the data word are set to '1'

bits 4, 5, 6 and 7 will be loaded into Data Register 120B or Data Register 120G respectively. Further, as described above, two or all three of bits 1, 2 and 3 may be set to '1' to simultaneously load bits 4, 5, 6 and 7 into more than one Data Register 120.

Depending upon which Data Register(s) 120 are loaded, the brightness of the light element 48 associated therewith is varied according to the received data.

Finally, the tenth (reset) CLOCK pulse is received and control unit 44 is ready to commence another transmission reception cycle.

Many uses are contemplated for the present invention. In particular, it is believed that the present invention will be suited for use in decorative lighting systems such as Christmas lighting. Figures 7, 8 and 9 show a decorative lighting module 200 which is currently contemplated for use in Christmas and other decorative lighting systems.

Decorative lighting module 200 comprises a control unit 44, a light element assembly 210, a wire clamp 214 and a locking nut 218. Light assembly 210 further comprises three light elements 222R, 222B and 222G and a diffusion lens 226. Light element 222R emits red light, while light elements 222B and 222G emit blue and green light respectively. Diffusion lens 226 operates to diffuse the light emitted by the light elements 222 such that, to an observer's eye, the light elements 222 appear as a single light source.

Light assembly 210 is removably coupled to control unit 44 by locking nut 218 which allows replacement of light assembly 210 in the event of failure of one or more light elements 222. Further, four

electrical connectors 230 electrically couple light elements 222 to control unit 44 in a removable fashion. Connectors 230 are received in complementary sockets 232 in control unit 44.

Control unit 44 is connected to a four conductor cable 238, shown in ghosted line in Figure 7, which comprises electrical connectors 52 and 56. As seen in the Figure, cable 238 also includes a key portion 242 which is received in keyway 246 of wire clamp 214 to assure correct orientation of electrical connectors 52 and 56 with respect to complementary electrical connection points 252 and 256 on control unit 44. The control unit 44 which is located nearest control system 40 would be unique within the system in that it also includes Voltage Conversion block 96.

As will be apparent, control unit 44 of decorative lighting module 200 does not include gate amplifiers 90 as it is contemplated that in many circumstances these will not be required. However, if gate amplifiers 90 are required due, for example to long runs of connectors 56, control unit 44 may be modified to include gate amplifiers 90 in any suitable manner as would be apparent to those of skill in the art. For example, incoming connectors 56 would be joined to one side of control unit 44 and outgoing connectors 56 would be connected to the output of gate amplifier 90 at other side of control unit 44 in a 'make and break' fashion.

It is contemplated that for most decorative lighting requirements, control units 44 will be sold in sets and each control unit 44 in a set will have a unique preset Unit ID. A consumer can therefore initially purchase a set of ten modules, twenty modules, etc. as meets his current needs. To allow the consumer to subsequently buy additional modules

without the risk of having non-unique Unit IDs, each control unit 44 includes six jumper sockets 280 with which the Group ID for the unit 44 may be set. Thus, the consumer need only insert jumpers 100 into one or more of jumper sockets 280 to select a unique Group ID for his subsequently purchased modules. this will allow the sale and use of sets of modules with Unit IDs which are preset by allowing for unique Group IDs to be established as required by the user.

Another contemplated use of the present invention is to construct illuminated display signs for advertising or other purposes. Figure 10 shows a display sign 300 constructed of an array of twenty-two rows of twenty-eight light modules 200. Each light module 200 comprises one pixel in the desired illuminated display and, due to the different coloured light elements in each module 200, each pixel may assume any one of several thousand different colours. While the Figure shows a simple 'happy face' character, it will be understood by those of skill in the art that more complex and/or animated displays may be produced simply by providing control system 40 with an appropriate program of data words.

In one contemplated embodiment of an illuminated display sign in accordance with the present invention, the signs will be installed in various public locations and their use will be leased to various advertisers. At the end of the lease term, the program of data words in control system 40 will be replaced with a new program. Such programs may be conveniently contained in one or more semiconductor memory devices which are removably connected to control system 40 as required.

Another contemplated use of the present invention is in automotive lighting. For example, instead of running eight or more

wires to an automotive tail light assembly, one or more light modules in accordance with the present invention may be installed in the tail light assembly requiring a maximum of four wires to be run. In this intended use, each light element 48 of a module may be placed in various portions of the tail light assembly as required. Further, if required, light elements 48R, 48B, 48G may be different colours as described above, or may be the same colour. For example, light element 48R may be a red brake light while light element 48B may be a white backup light and light element 48G may be a red turn signal.

Other uses and variations of the present invention will occur to those of skill in the art and should not be considered as departing from the scope of the present invention as defined in the claims as appended hereto.

What is claimed is:

1. A controlled lighting system comprising:

a control system;

a plurality of light modules, each module including at least two light elements;

a control unit for each light module receiving control signals from said control system and independently operating each of said at least two light elements in response to said control signals, each control unit operating in response to a unique control signal.

2. A controlled lighting system according to claim 1 wherein said control signals are received from said control system by said control units through one or more control networks.

3. A controlled lighting system according to claim 1 wherein the voltage applied to each of said at least two light elements is altered by said control unit in response to said control signals.

4. A controlled lighting system according to claim 1 wherein each of said at least two light elements is removably connected to said control unit.

5. A controlled lighting system according to claim 1 wherein said at least two light elements are formed in a light module which is removably connected to said control unit.

6. A controlled lighting system according to claim 5 wherein said light module further includes means to blend the light emitted by each said light element.

7. A controlled lighting system according to claim 1 wherein said control system comprises a microcomputer controller.

8. A controlled lighting system according to claim 1 wherein said control system comprises at least one light sensor responsive to the light received at the sensor and means responsive to said at least one light sensor to supply control signals to alter the light received at the sensor.

9. A controlled lighting system according to claim 2 wherein each control unit includes a unique address within said control network.

10. A controlled lighting system according to claim 9 wherein said control signals comprise signals indicating to said control unit said unique address, at least one of said at least two light elements and a desired output level for said at least one of said at least two light elements.

11. A light module comprising:

a housing;

at least two light elements within said housing, each light element emitting light of a different wavelength;

means to blend the light emitted by each said light element;

a control unit including address decoding means to compare an address received at said control unit with a unique address pre-assigned to said control unit, said control unit being responsive to signals with said unique address to vary the light emitted by each said light element.

12. A light module according to claim 11 further wherein said means to blend the light comprises a diffusion lens.

13. A light module according to claim 11 including at least three light elements each light element emitting a different one of the primary additive colours.

14. A light module according to claim 11 wherein said housing is removably connected to said control unit.

15. An illuminated display comprising:

a support;

a control system;

a plurality of light modules arranged in an array on said support, each light module including at least two light elements and a control unit to independently alter the amount of light emitted by each of said light elements in response to control signals received from said control system, wherein said control system transmits a predefined sequence of control signals to said light modules to illuminate said light elements of said light modules to produce a desired display.

16. An illuminated display according to claim 15 wherein said control system transmits a predetermined series of sequences of control signals to alter the illumination of said light elements of said light modules to animate said desired display.

17. An illuminated display according to claim 15 wherein said control system includes a means for storing said predefined sequences of control signals, said control system retrieving and transmitting the stored predefined sequences of control signals.

18. An illuminated display according to claim 17 wherein said means for storing said predefined sequences of control signals comprises a removable integrated circuit.

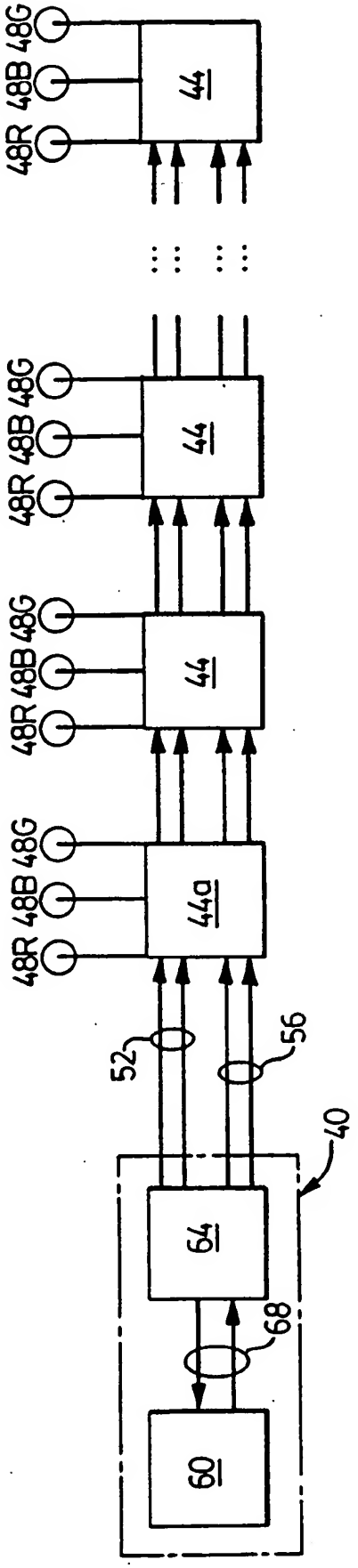

FIG. 1

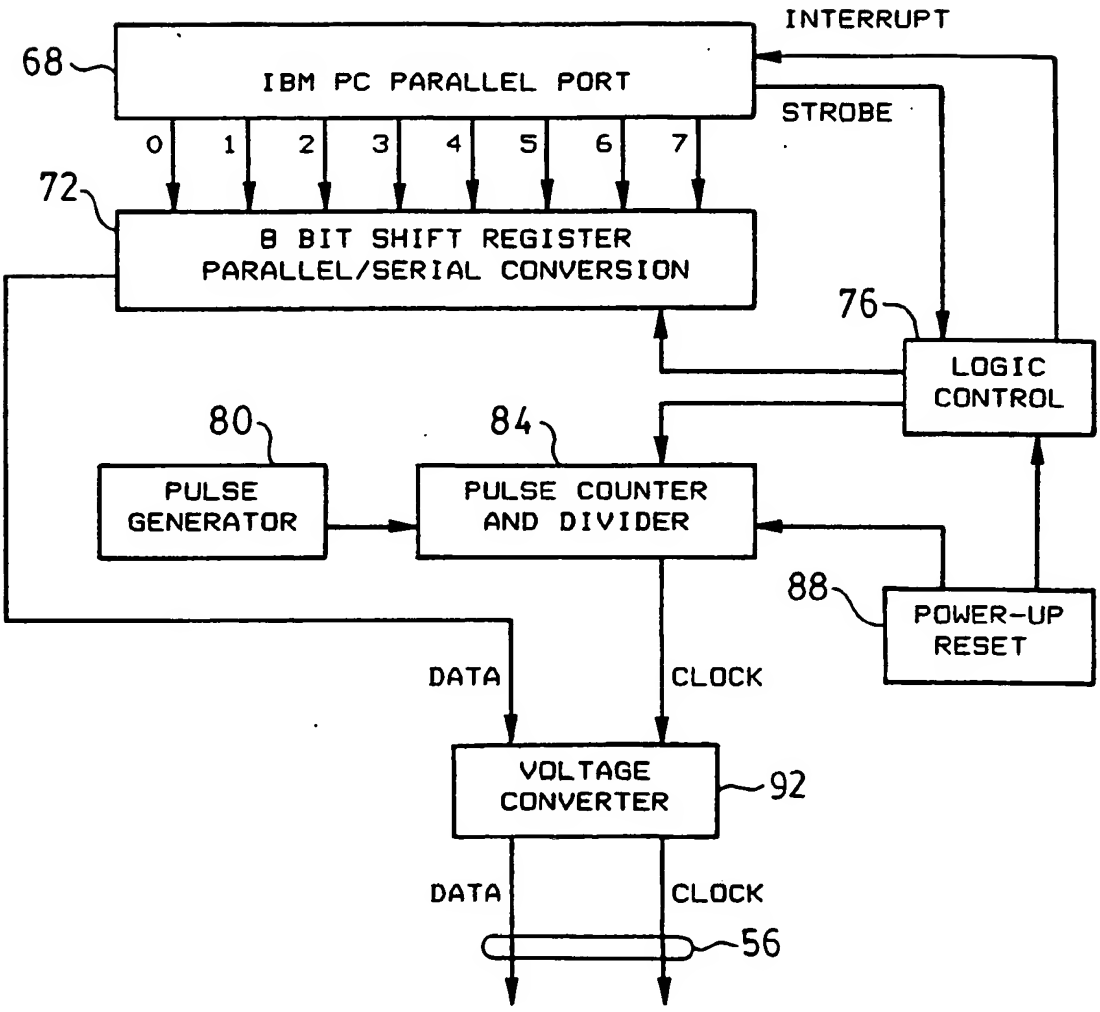
INTERRUPT
68
IBM PC PARALLEL PORT
STROBE
0
1
2
3
4
5
6
7
72
8 BIT SHIFT REGISTER
PARALLEL/SERIAL CONVERSION
76
LOGIC
CONTROL
80
84
PULSE
GENERATOR
PULSE COUNTER
AND DIVIDER
88
POWER-UP
RESET
DATA
CLOCK
VOLTAGE
CONVERTER
92
DATA
CLOCK
56

FIG. 2

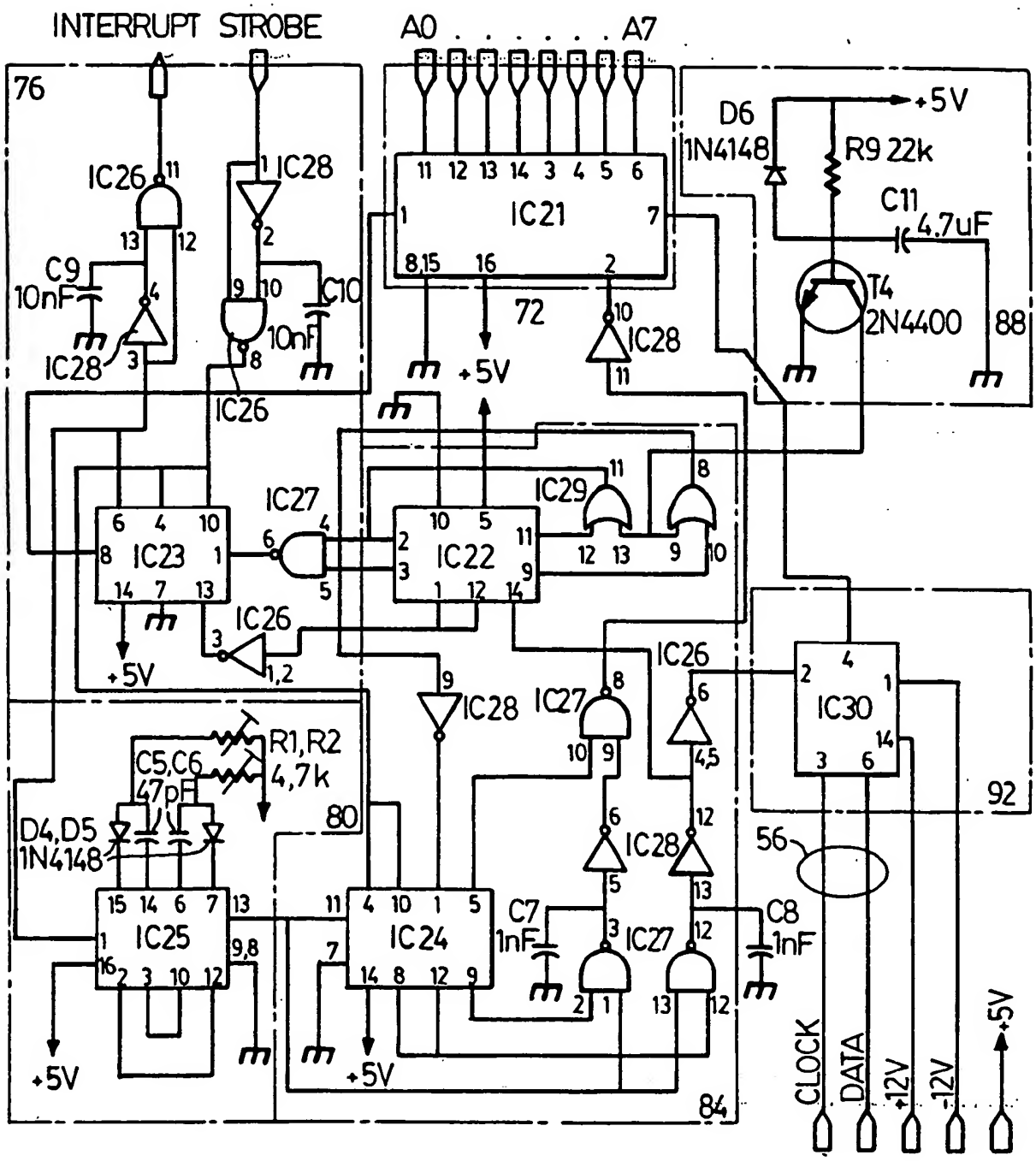
INTERRUPT STROBE
A0 . . . . . A7
76
IC26
IC28
C9
10nF
C10
10nF
IC21
72
+5V
D6
1N4148
R9 22k
C11
4.7uF
T4
2N4400
88
IC23
IC22
IC27
IC29
IC30
92
R1,R2
4,7k
C5,C6
47pF
80
D4,D5
1N4148
IC25
IC24
C7
1nF
C8
1nF
56
84
CLOCK
DATA
+12V
-12V
+5V

FIG. 3

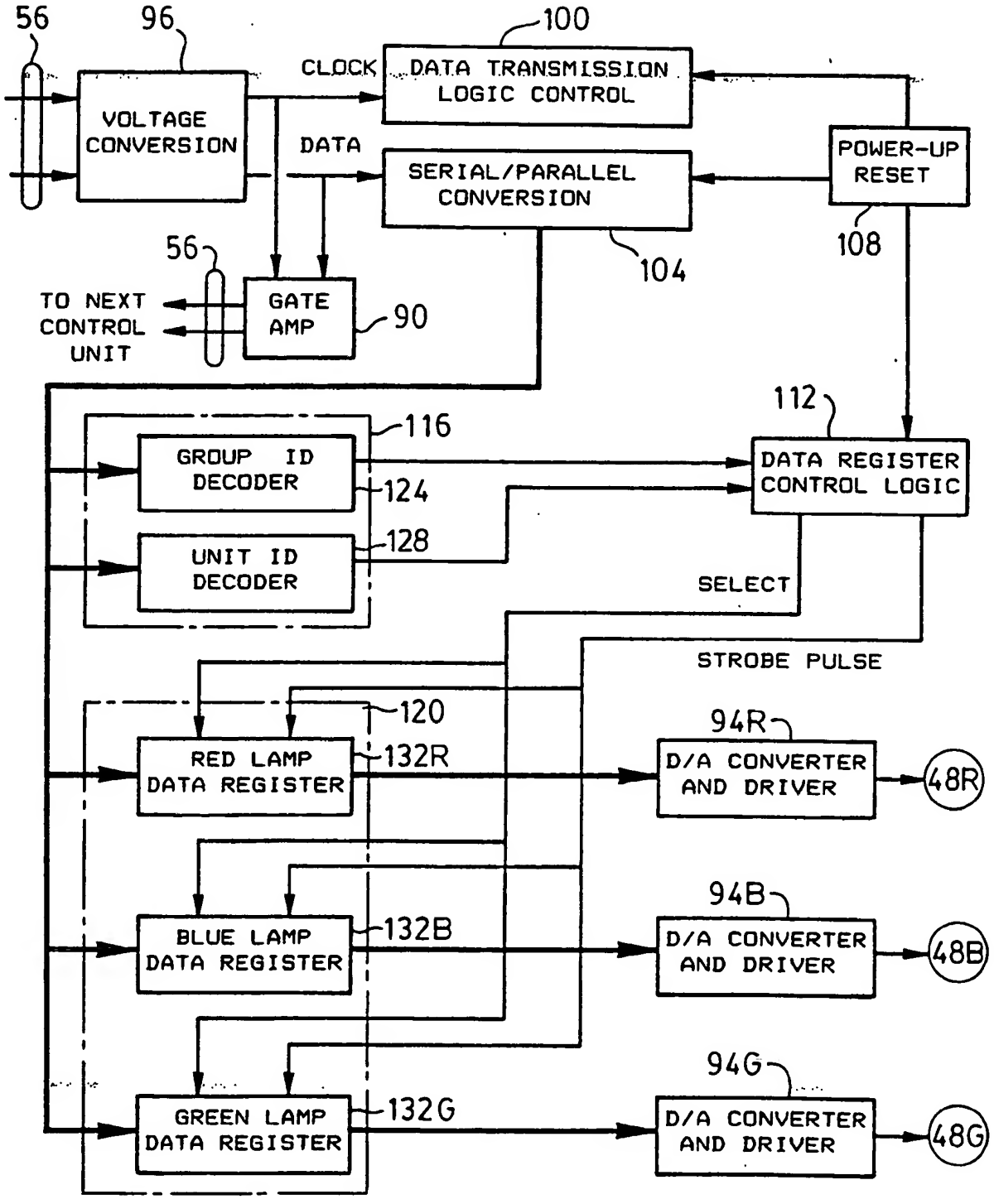
56
96
100
CLOCK
DATA TRANSMISSION LOGIC CONTROL
VOLTAGE CONVERSION
DATA
SERIAL/PARALLEL CONVERSION
POWER-UP RESET
108
104
56
TO NEXT CONTROL UNIT
GATE AMP
90
112
116
GROUP ID DECODER
124
DATA REGISTER CONTROL LOGIC
UNIT ID DECODER
128
SELECT
STROBE PULSE
120
94R
RED LAMP DATA REGISTER
132R
D/A CONVERTER AND DRIVER
48R
94B
BLUE LAMP DATA REGISTER
132B
D/A CONVERTER AND DRIVER
48B
94G
GREEN LAMP DATA REGISTER
132G
D/A CONVERTER AND DRIVER
48G

FIG. 4

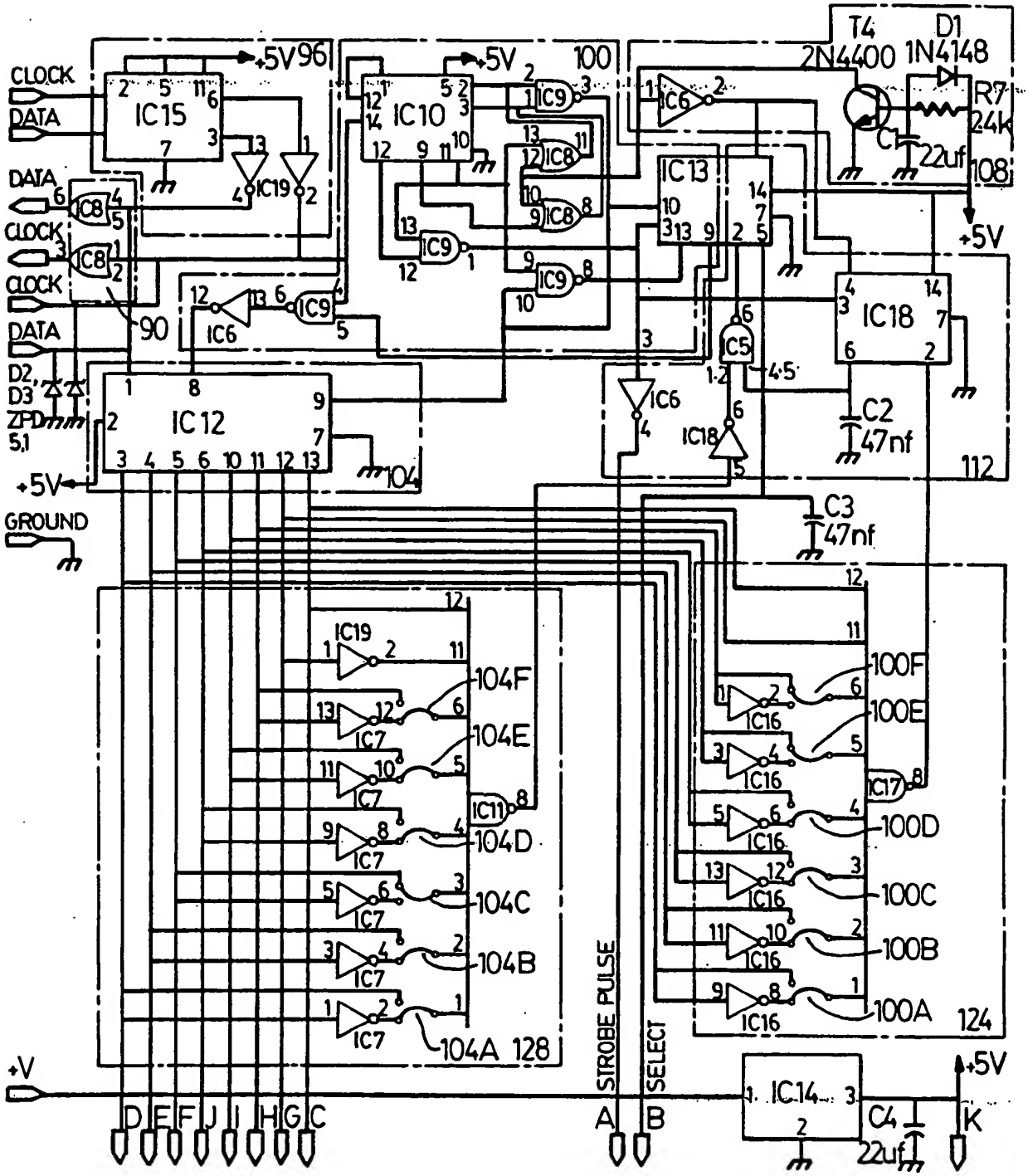
CLOCK
DATA
DATA
CLOCK
CLOCK
DATA
D2
D3
ZPD
5,1
GROUND
+V
+5V
IC15
IC10
IC12
IC13
IC18
IC19
IC6
IC8
IC9
IC5
IC16
IC17
IC14
T4
2N4400
D1
1N4148
R7
24k
C1
22uf
C2
47nf
C3
47nf
C4
22uf
90
100
104
108
112
124
128
104F
104E
104D
104C
104B
104A
100F
100E
100D
100C
100B
100A
STROBE PULSE
SELECT
D E F J I H G C
A B
K

FIG. 5

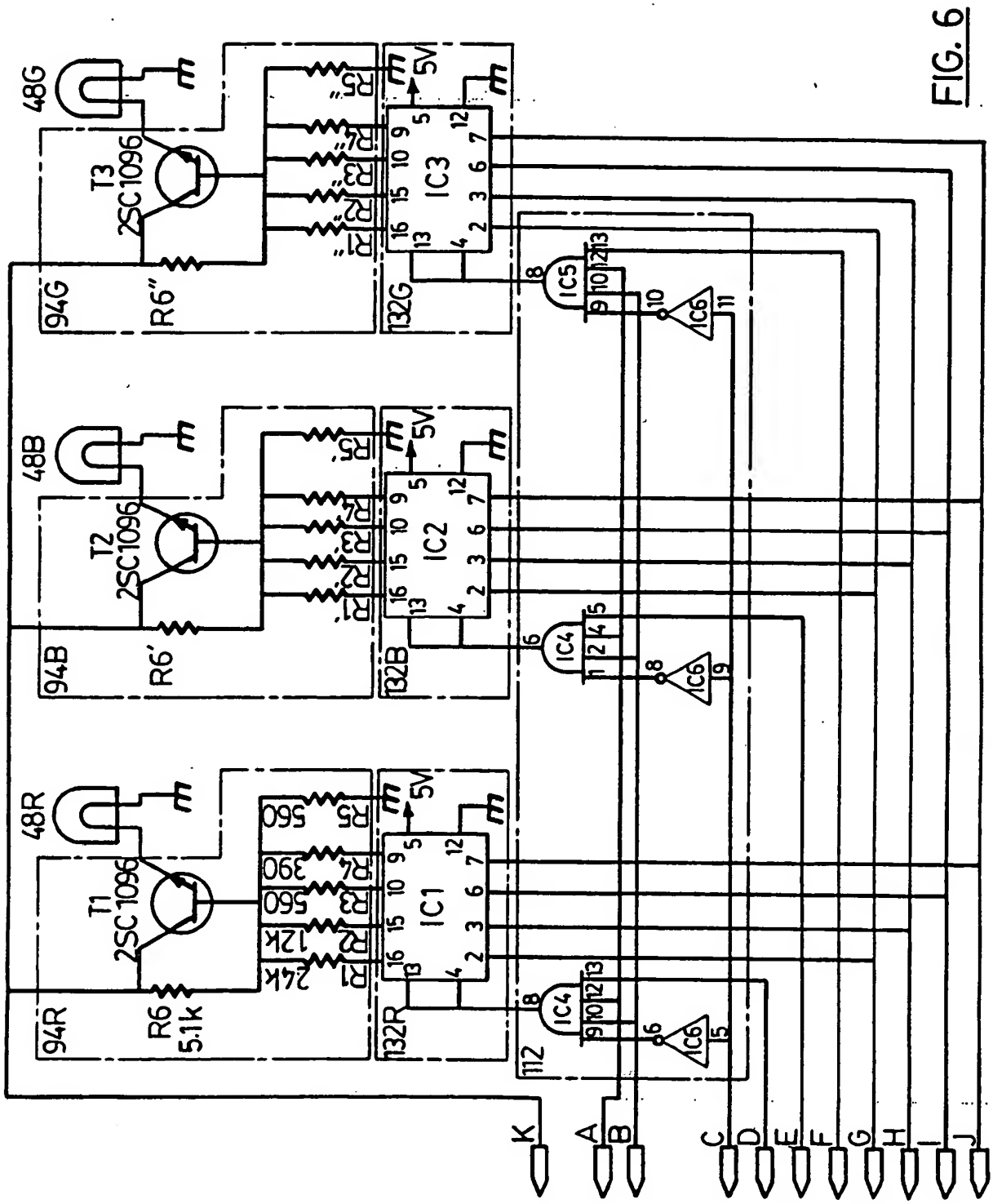
48G
T3
2SC1096
94G
R6"
132G
IC3
5V
48B
T2
2SC1096
94B
R6'
132B
IC2
48R
T1
2SC1096
94R
R6
5.1k
132R
IC1
560
390
560
12K
24K
IC5
IC4
IC6
112
K
A
B
C
D
E
F
G
H
J

FIG. 6

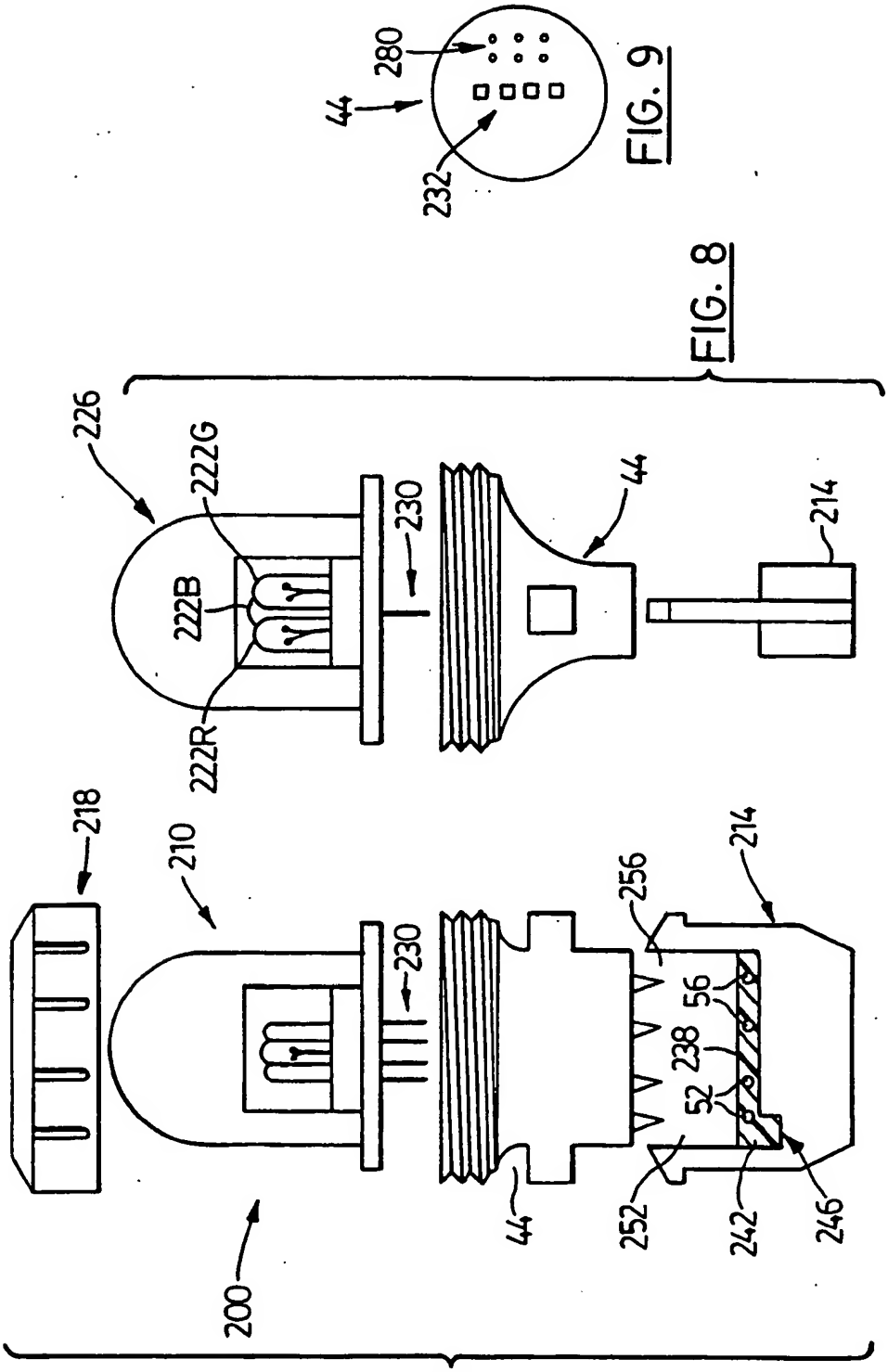

FIG. 7

FIG. 8

FIG. 9

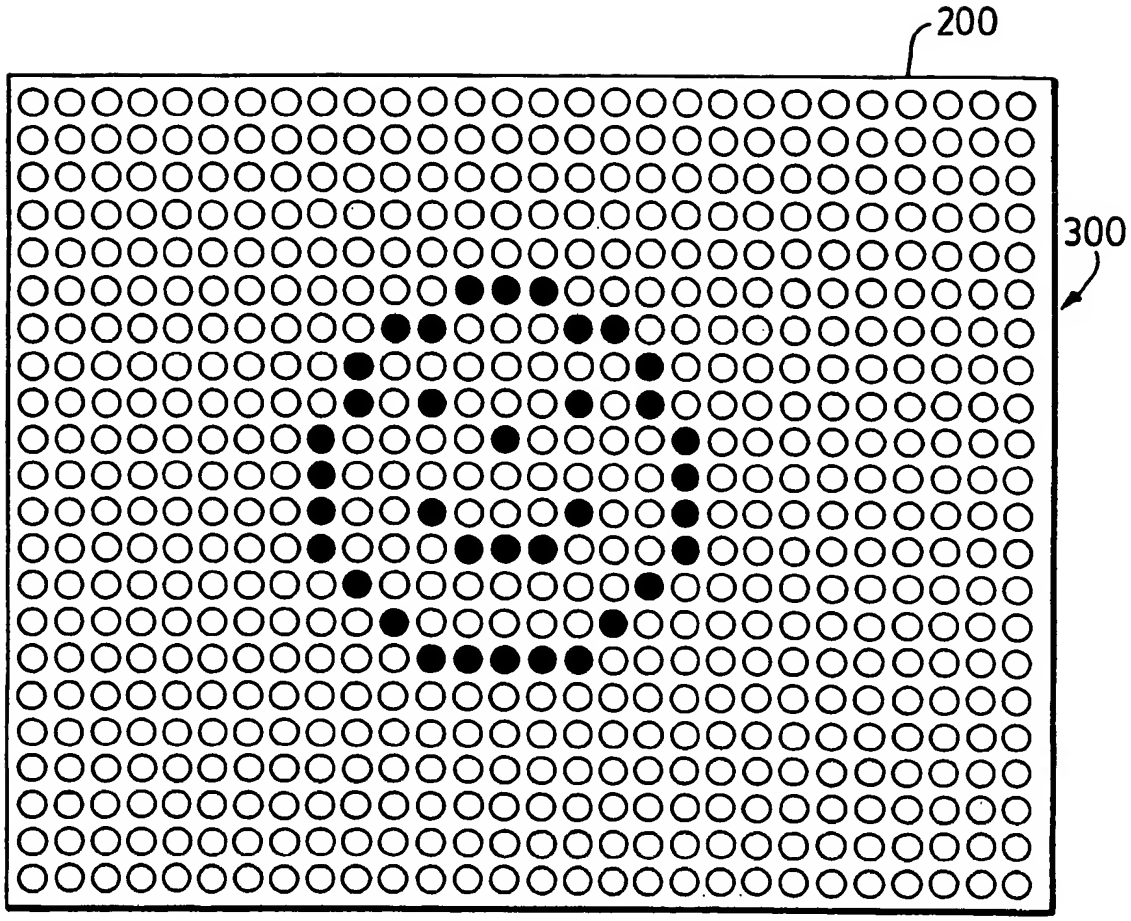

FIG 10

INTERNATIONAL SEARCH REPORT

Information on patent family members

28/05/94

International application No.
PCT/CA 94/00078

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 4388567	14/06/83	GB-A,B- 2070830	09/09/81
		JP-C- 1474466	18/01/89
		JP-A- 56118295	17/09/81
		JP-B- 63024317	20/05/88
US-A- 4559535	17/12/85	NONE	
DE-A1- 3917101	29/11/90	NONE	

A. CLASSIFICATION OF SUBJECT MATTER

IPC : H05B 37/02
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC : F21S, G09G, H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, CLAIMS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 4388567 (TOSHIBA ELECTRIC EQUIPMENT CORPORATION), 14 June 1983 (14.06.83), see the whole document --	1-18
A	US, A, 4559535 (SIGMATRON NOVA, INC.), 17 December 1985 (17.12.85), column 3, line 25 - column 10, line 66, figures 1-12 --	11-18
A	DE, A1, 3917101 (WOLFGANG RIENECKER), 29 November 1990 (29.11.90), column 3, line 18 - column 5, line 38, figure 1 --	1-18

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
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Date of the actual completion of the international search	Date of mailing of the international search report
21 June 1994	- 8. 07. 94

Name and mailing address of the International Searching Authority:
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BERTIL NORDENBERG

Form PCT/ISA/210 (second sheet) (July 1992)